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**EUROPEAN PATENT APPLICATION**

21 Application number: 89202768.1

51 Int. Cl.<sup>5</sup>: H03K 3/023, H03F 1/02

22 Date of filing: 03.11.89

30 Priority: 07.11.88 NL 8802719

43 Date of publication of application:  
16.05.90 Bulletin 90/20

84 Designated Contracting States:  
CH DE FR GB IT LI

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54 Delay-controlled relaxation oscillator with reduced power consumption.

57 A capacitance (10) in an oscillator is alternately charged and discharged. The change-over from charging to discharging is controlled by means of a comparator (22) which compares a capacitance voltage (20) with a reference voltage ( $V_{ref}$ ). The oscillator comprises switching means (40, 42) for switching the power supply for the comparator from a power supply mode into a stand-by mode between two change-overs.

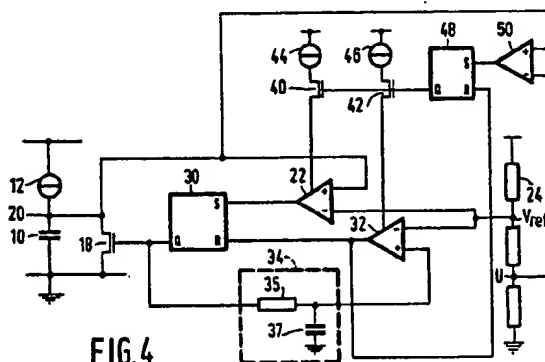


FIG.4

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# **Delay-controlled relaxation oscillator with reduced power consumption.**

The invention relates to an oscillator including:

- a capacitance;
- a charging means for charging the capacitance;
- a discharging means for discharging the capacitance;
- a control comparator for comparing a capacitance voltage, representative of a degree of charge at the capacitance, with a reference voltage;
- a monostable multivibrator means having a control input coupled with a control comparator output for activating the discharge means for a predetermined time interval.

An oscillator of this kind is known from the European Patent Application EP-A- 147 810. In order to enable fast switching, the gain of said control comparator should be high. Consequently, the control comparator has a correspondingly high power consumption. However, the control comparator is indispensable only during a time interval around a change-over from charging to discharging of the capacitance and a change-over from discharging to charging of the capacitance. Outside these intervals the monostable multivibrator means ensures that the discharging means remains in the desired conductive or blocked state.

It is therefore an object of the invention to provide an oscillator of the afore-mentioned type having a reduced power consumption with regard to the prior art oscillator.

An oscillator according to the invention is therefore characterized in that the oscillator further includes switching means for switching a power supply for the control comparator into a stand-by mode at least after a change-over from charging to discharging of the capacitance or after a change-over from discharging to charging, and into an operating mode at least before a change-over from discharging to charging, or before a change-over from charging to discharging, respectively. The switching between a stand-by mode (low power) and an operating mode (high power), for instance under control of the oscillator signal itself, enables a simple way of reducing power consumption.

In an embodiment of an oscillator in accordance with the invention characterized in that the control comparator includes a transistor differential pair being fed by a parallel arrangement of a constant current source and a controllable current source that is controlled by the switching means. In the stand-by mode the controllable current source remains turned off and in the operating mode the controllable current source remains turned on. The controllable current source and the constant current source together may comprise a parallel arrangement of conduction channels of two

transistors that have their conduction channels coupled with a common node of the transistor differential pair.

The switching means may comprise

- a switching means comparator for comparing the capacitance voltage with a second reference voltage differing from said reference voltage, referred to hereinafter as first reference voltage.

The values of the reference voltages determine the moment at which the switching between the modes occurs.

A further embodiment of an oscillator according to the invention is characterized in that the monostable multivibrator means comprises:

- a set-reset flip-flop means having a set input coupled with the control comparator output;
- a further control comparator for comparing a further voltage, associated with a delayed version of said capacitance voltage, with the reference voltage, having a further control comparator output coupled with a reset input of said flip-flop means, while the switching means controls a power supply for both the control comparator and the further control comparator.

By using a further control comparator in addition to the first-mentioned control comparator the set-reset flip-flop is controlled by control signals that have accurately defined transitions. Both control comparators are powered through the switching means.

A further embodiment of an oscillator in accordance with the invention is characterized in that the switching means comprises:

- a switching means comparator for comparing the capacitance voltage with a second reference voltage differing from said reference voltage, referred to hereinafter as the first reference voltage;
- a further set-reset flip-flop means having a set input coupled to a switching means comparator output and having a reset input coupled with the reset input of the first-mentioned set-reset flip-flop, a further flip-flop output thereof controlling the power supply for both the control comparator and the further control comparator. Preferably, the switching means comparator is small as compared with the control comparators for the switching time of the switching means comparator has no effect on the duration of the oscillation period.

Thus, oscillators are realised which have an accurately defined oscillation period and a low power consumption.

The invention will be described in detail hereinafter with reference to a drawing; therein

Fig. 1 shows the circuit diagram of a known oscillator,

Figs. 2A, 2B and 2C show embodiments of

an oscillator realized in accordance with an aspect of the invention.

Figs. 3A, 3B and 3C show embodiments of an oscillator in accordance with the principle shown in Fig. 1, and

Fig. 4 shows a preferred embodiment of an oscillator in accordance with the invention.

Fig. 1 shows the circuit diagram of a known oscillator. The oscillator shown comprises a series connection of a capacitance 10 and a current source 12 between power supply terminals 14 and 16. A current channel of a transistor 18 is connected parallel across the capacitance 10. The node 20 between the capacitance 10 and the current source 12 is connected to a non-inverting input of a comparator 22, an inverting input of which is connected to a voltage divider 24 for supplying a reference voltage  $V_{ref}$ . A control electrode of the transistor 18 is connected to the comparator output via delay means 26. The delay means 26 turn off the transistor 18 a predetermined period of time after the transistor has been turned on. Due to the current applied to the capacitance the voltage on the node 20 increases until it reaches a value which is substantially equal to the reference voltage. At that instant the voltage on the comparator output changes from low to high and the transistor 18 is turned on, with the result that the capacitance 10 is discharged. The delay means ensure that the transistor 18 remains turned on for a predetermined period of time in order to ensure that the voltage on the node 20 decreases sufficiently, for example to one per thousand of the maximum capacitance voltage. When the transistor 18 is subsequently turned off again, the voltage on the node 20 can increase again until the next discharge occurs. It is to be noted that, even though the symbol of a current source is used in Fig. 1, it is to be understood to include also a resistance. It is also to be noted that, for example a further resistance can be inserted in the discharging path in order to impart a less steep negative-going edge to a sawtooth voltage across the capacitance 10.

Figs. 2A, 2B and 2C show embodiments of an oscillator in accordance with an aspect of the invention. The components which correspond to components shown in Fig. 1 are denoted by the same reference numerals.

In Fig. 2A the delay means comprise an RS flip-flop 30, a second comparator 32 and a delay element 34. The output of the first comparator 22 is connected to the set input of the flip-flop 30. The second comparator 32 comprises an output which is coupled to the reset input of the flip-flop 30. The inverting inputs of the comparators 22 and 32 are connected to one another and to a reference voltage  $V_{ref}$ . The non-inverting input of the comparator 32 is coupled, via the delay element 34, to the non-

inverting output of the flip-flop 30. The delay element 34 comprises, for example a temperature-stabilized combination of a resistance and a further capacitance, the latter capacitance connecting the non-inverting input of the comparator 32 to the power supply terminal 16. Alternatively, the delay element 34 comprises, for example a number of cascade-connected inverters. Another possibility consists in that the delay element 34 comprises a semiconductor delay line, a square root of the resistance and capacitance thereof defining the delay. Preferably, the delay element 34 has a low temperature sensitivity.

The operation of the circuit is as follows. As soon as the capacitance voltage on the node 20 exceeds the reference voltage  $V_{ref}$ , the flip-flop 30 is set by the comparator 22 so that the flip-flop output turns on the transistor 18 by way of a high signal. Subsequently, the voltage on the node 20 decreases. The comparator 22 then applies a low signal to the set input. The output voltage of the flip-flop 30 does not change in response thereto. The output voltage is applied, via the delay element 34, to the comparator 32 which supplies the reset input of the flip-flop 30 with a high signal after a predetermined period of time. Subsequently, the flip-flop 30 is reset and the transistor 18 is turned off by means of a low output signal of the flip-flop. The circuits shown in the Figs. 2B and 2C deviate from the circuit shown in Fig. 2A merely in that the signal is applied to the second comparator 32 in a delayed fashion or originates from the output of the comparator 22 and from the node 20. Provided that this signal has the correct polarity and is indicative of the voltage on the node 20, either directly or indirectly, the latter two circuits operate in the same way as the circuit shown in Fig. 2A. However, it may be that the use of an as small as possible delay element 34 is to be preferred. Therefore, it is advantageous to utilize the inherent switching delay of the flip-flop 30 and to connect the delay element 34 to the output of the flip-flop 30.

Fig. 2 utilizes two comparators in order to ensure that the flip-flop 30 is controlled by means of well-defined control signals. This benefits the accuracy of the oscillation period.

The Figs. 3A, 3B and 3C show embodiments of an oscillator in accordance with the principle of Fig. 1. Components which correspond to components of the circuits shown in the preceding Figures are denoted by the same reference numerals.

The circuits shown in the Figs. 3A, 3B and 3C require only a single comparator 22. The reset input of the flip-flop 30 is now fed directly via the delay element 34. In practice delay elements are often frequency-selective, so that a sharp transition of a signal applied to such a delay element 34 is distorted. This could introduce some inaccuracy as

regards the instant of switching of the flip-flop 30. By the addition of an additional comparator as in the Figs. 2A, 2B and 2C, this problem can be mitigated. However, this has the drawback that the current consumption is higher and that the dimensions of the circuit are larger. The circuits shown in the Figs. 3A, 3B and 3C deviate from one another in the same way as the circuits shown in the Figs. 2A, 2B and 2C, i.e. in that the signal applied to the flip-flop 30 via the delay element 34 is derived from different points in the circuit.

Fig. 4 shows a preferred embodiment of an oscillator in accordance with the invention. Components which correspond to components of the preceding Figures are denoted by the same reference numerals. The delay element 34 is constructed as an RC combination comprising a resistance 35 and a capacitance 37. Comparators 22 and 32 are connected, via switches 40 and 42, to a power supply source which is in this case represented by the current sources 44 and 46. For as long as these switches are blocked, the comparators are connected to a stand-by power supply (not shown). To this end, each of the comparators 22 and 32 comprises, for example a differential amplifier of a long-tailed pair type which is powered by a stand-by current source in the tail. As soon as the switches 40 and 42 are conductive, a power supply source is connected parallel to the stand-by current source so that the currents in the differential amplifier increase. The switches 40 and 42 are coupled to an output of a flip-flop 48, a set input of which is connected to an output of the comparator 50 and a reset input of which is coupled to the output of the comparator 32. An inverting input of the comparator 50 receives a reference voltage U which is lower than the reference voltage  $V_{ref}$ . The non-inverting input of the comparator 50 is connected to the node 20 which carries the capacitance voltage. Before the capacitance voltage equals the reference voltage U, the switches 40 and 42 are blocked. At the instant at which the capacitance voltage exceeds the reference voltage U, the power supply source 44 and 46 are connected to the comparators 22 and 32. The capacitance voltage subsequently increases until it reaches the level  $V_{ref}$ . As has already been described, the capacitance 10 is subsequently discharged via the transistor 18 which remains turned on until the comparator 32 resets the flip-flop 30 by way of a high signal. At that instant the flip-flop 48 is also reset, so that the power supply is switched off. Thus, the comparators 22 and 32 dissipate power only when the transistor 18 switches.

## Claims

### 1. Oscillator including:

- a capacitance;
  - a charging means for charging the capacitance;
  - a discharging means for discharging the capacitance;
  - a control comparator for comparing a capacitance voltage, representative of a degree of charge at the capacitance, with a reference voltage;
  - a monostable multivibrator means having a control input coupled with a control comparator output for activating the discharge means for a predetermined time interval;
- characterized in that the oscillator further includes switching means for switching a power supply for the control comparator into a stand-by mode at least after a change-over from charging to discharging of the capacitance or after a change-over from discharging to charging, and into an operating mode at least before a change-over from discharging to charging, or before a change-over from charging to discharging, respectively.

2. Oscillator as claimed in Claim 1, characterized in that the control comparator includes a transistor differential-pair being fed by a parallel arrangement of a constant current source and a controllable current source that is controlled by the switching means.

3. Oscillator as claimed in Claim 1 or 2, characterized in that the switching means comprises:

- a switching means comparator for comparing the capacitance voltage with a second reference voltage differing from said reference voltage, referred to hereinafter as first reference voltage.

4. Oscillator as claimed in Claim 1 or 2, characterized in that the monostable multivibrator means comprises:

- a set-reset flip-flop means having a set input coupled with the control comparator output;
- a further control comparator for comparing a further voltage, associated with a delayed version of said capacitance voltage, with the reference voltage, having a further control comparator output coupled with a reset input of said flip-flop means, while the switching means controls a power supply for both the control comparator and the further control comparator.

5. Oscillator as claimed in Claim 4, characterized in that a delay element is disposed in one of the following paths:

- a first path between a flip-flop output and a further control comparator input;
- a second path between the control comparator output and the further control comparator input;
- a third path between a control comparator input and the further control comparator input.

6. Oscillator as claimed in Claim 4, characterized in that the switching means comprises:

- a switching means comparator for comparing the

capacitance voltage with a second reference voltage differing from said reference voltage, referred to hereinafter as the first reference voltage;

- a further set-reset flip-flop means having a set input coupled to a switching means comparator output and having a reset input coupled with the reset input of the first-mentioned set-reset flip-flop, a further flip-flop output thereof controlling the power supply for both the control comparator and the further control comparator.

7. Oscillator as claimed in Claim 3 or 4, characterized in that the switching means comparator is substantially smaller than each of said control comparators.

8. Oscillator including:

- a capacitance;
- a charging means for discharging the capacitance;
- a discharging means for discharging the capacitance;
- a control comparator for comparing a capacitance voltage, representative of a degree of charge at the capacitance, with a reference voltage;
- a monostable multivibrator means having a control input coupled with a control comparator output for activating the discharge means for a predetermined time interval;

characterized in that the monostable multivibrator means includes:

- a set-reset flip-flop means having a set input coupled with the control comparator output;
- a further control comparator for comparing a further voltage, associated with a delayed version of said capacitance voltage, with the reference voltage, having a further control comparator output coupled with a reset input of said flip-flop means.

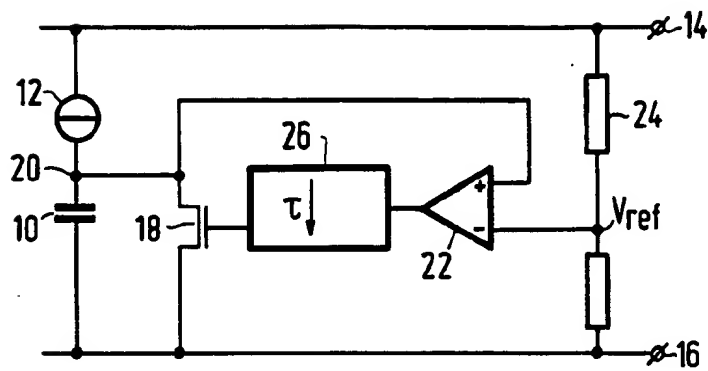


FIG. 1

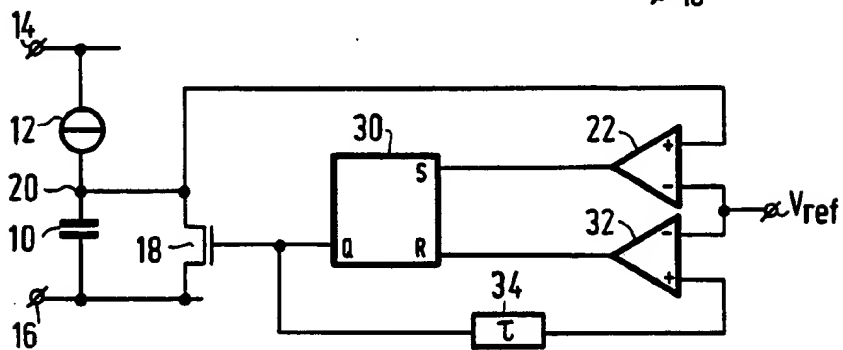


FIG. 2A

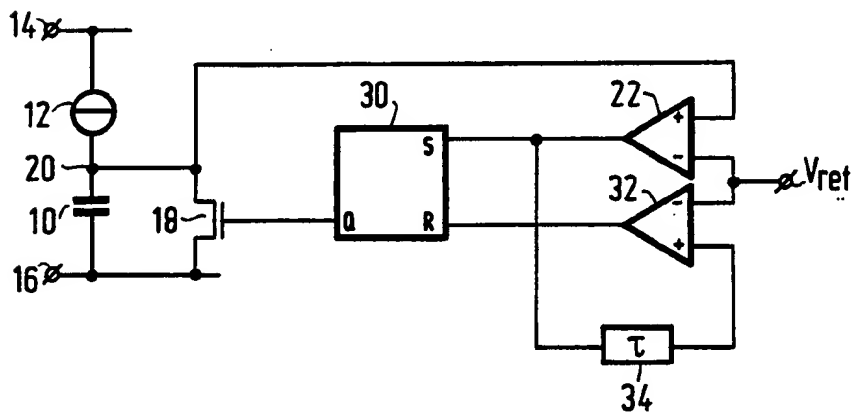


FIG. 2B

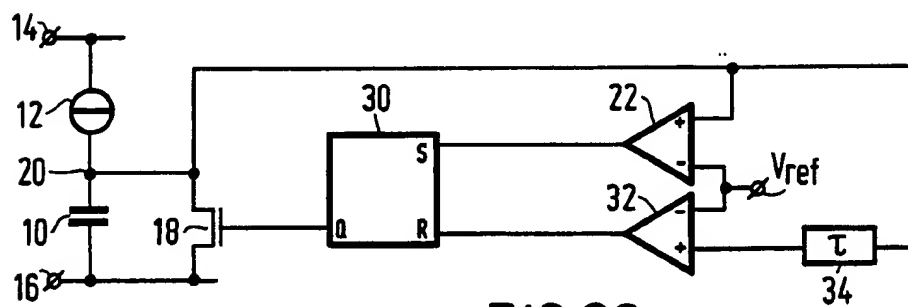


FIG. 2C

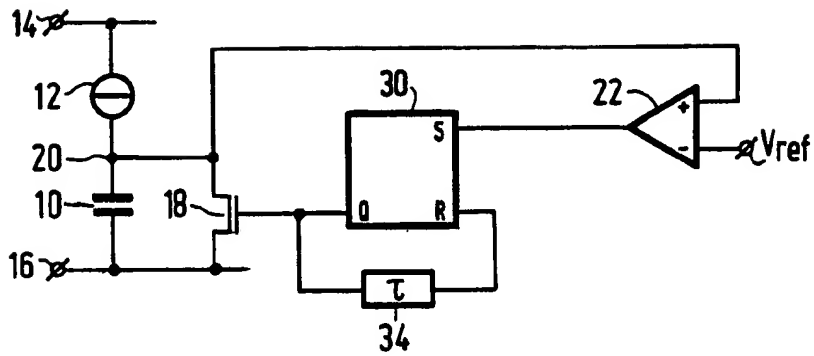


FIG. 3A

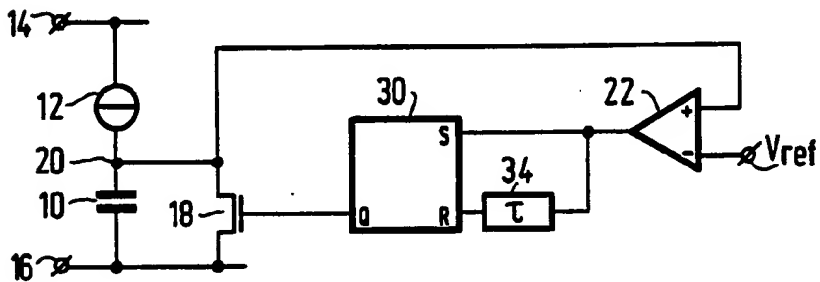


FIG. 3B

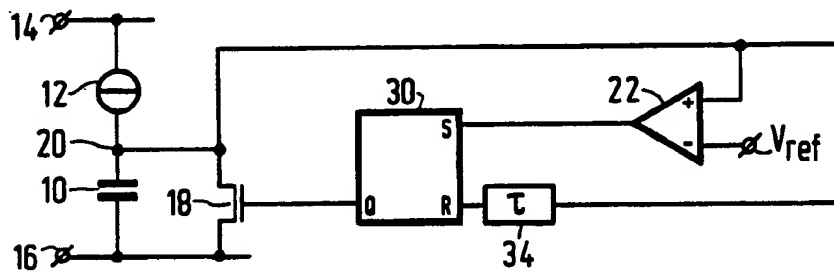


FIG. 3C

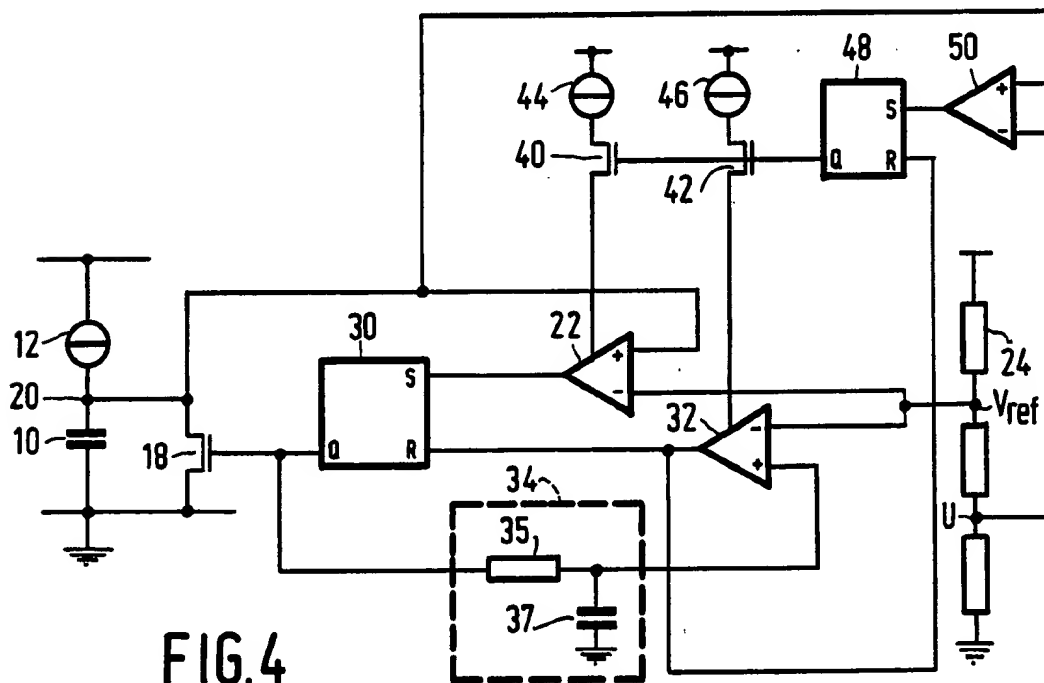


FIG. 4



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## EUROPEAN SEARCH REPORT

Application Number

EP 89 20 2768

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	EP-A-0 147 810 (TOSHIBA) * Page 10, last paragraph - page 14; figure 7 *	1,3	H 03 K 3/023 H 03 F 1/02
Y	--- US-A-4 472 688 (SABURO et al.) * Column 2, line 23 - column 3, line 39; figure 3 *	1,3	
A	---	4-6	
X	--- US-A-4 191 932 (NAGAHAMA) * Column 2, line 16 - column 3, line 20; column 4, lines 25-55; figures 1,5 *	8	
A	-----	1,4-6	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H 03 K H 03 F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 12-02-1990	Examiner CANTARELLI R.J.H.
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